INTERNATIONAL UNIVERSITY OF EAST AFRICA

'Learning to Succeed'

FACULTY OF ENGINEERING

END OF SEMESTER EXAMINATIONS - APRIL 2025

PROGRAMME: BACHELOR OF ELECTRICAL AND CONTROL ENGINEERING

YEAR/SEM: YEAR 2/SEMESTER 2

COURSE CODE: ELC2232

NAME: ANALOGUE ELECTRONICS II

DATE: 2025-04-23

TIME: 9:00AM-12:00PM

INSTRUCTIONS TO CANDIDATES:

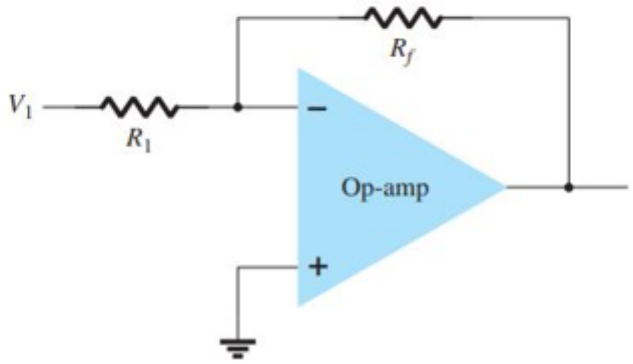
1. Read the instructions very carefully
2. The time allowed for this examination is STRICTLY three hours
3. Read each question carefully before you attempt and allocate your time equally between all the Sections
4. Write clearly and legibly. Illegible handwriting cannot be marked
5. Number the questions you have attempted
6. Use of appropriate workplace examples to illustrate your answers will earn you bonus marks
7. Any examination malpractice detected will lead to automatic disqualification.

DO NOT WRITE ANYTHING ON THE QUESTION PAPER

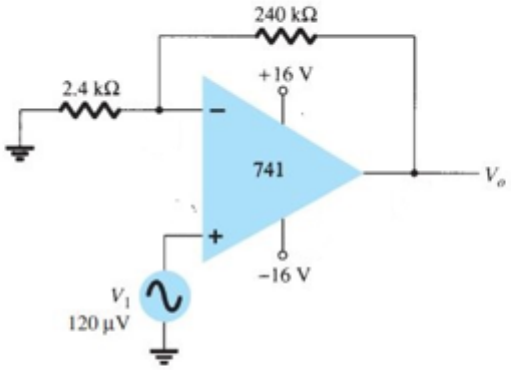
Section A Attempt any 2 questions in Section A

Question 1:

a. Explain the term *Gain, Common Mode rejection Ratio* and *slew rate* as applied to Operation amplifiers *(6 Marks)*
b. Explain the assumptions to be put in consideration for the operation of an ideal operational amplifier *(4 Marks)*
c. Consider the amplifier circuit below, Calculate the input voltage for the amplifier circuit for which the output voltage, $V_o = -10v$, $R_f = 500k\Omega$ and , $R_1 = 100k\Omega$ *(3 Marks)*



d. Calculate the output voltage V_o from the circuit of Figure below for an input of 120 mV *(3 Marks)*



e. A differential amplifier has an open-loop voltage gain of 120 and a common input signal of 3.0 V to both terminals. An output signal of 30mV results. Calculate the common-mode gain and the CMRR *(6 Marks)*

f. List any three (03) applications of operational amplifiers *(3 Marks)*

Question 2:

a) Outline four different classes of power amplifiers *(4 Marks)*

b) Considering Class, A amplifiers, outline 2 advantages and disadvantages of class A amplifiers *(4 Marks)*

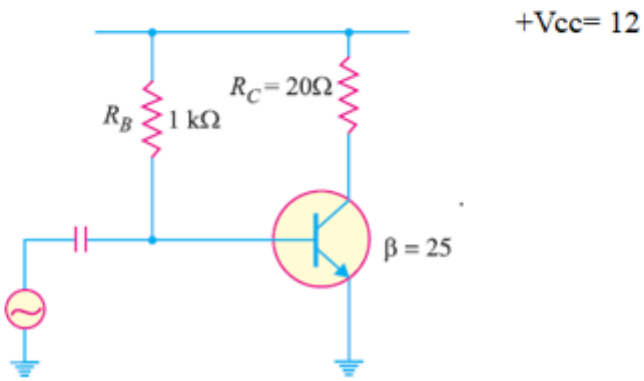
c) Calculate the

(i) Which class of power amplifier does the amplifier shown the below belong *(2 Marks)*

(ii) Output power *(5 Marks)*

(iii) Input power *(5 Marks)*

(iv) Collector efficiency of the amplifier circuit shown in Figure below. It is given that input voltage results in a base current of 10 mA peak. *(5 Marks)*



Question 3:

a. Explain the concept of *feedback (2 Marks)*
b. Distinguish between *Positive feedback* and Negative feedback *(2 Marks)*
c. List any three applications of the feedback in electronics *(3 Marks)*
d. Outline four characteristics of negative feedback *(4 Marks)*
e. Outline the four basic ways of connecting feedback circuits *(4 Marks)*
f. Sketch a simple circuit diagram of a voltage series Feedback circuit, indicate all relevant currents and voltages *(5 Marks)*
g. The voltage gain of an amplifier without feedback is *4000*. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. Given that feedback fraction $\beta = 0.02$. *(5 Marks)*

Question 4:

a. Define the terms Differential mode and Common mode as applied in operation amplifiers *(04 Marks)*
b. During an experiment figure a and b were obtained. Figure a shows the operation of the amplifier with a differential mode while figure b shows the operation of the circuit in common mode. Calculate the CMRR for the circuit measurements. Given $Vout = V_{dm}*(V_1-V_2) + V_{cm}* \frac{(V_1+V_2)}{2}$ *(08 Marks)*

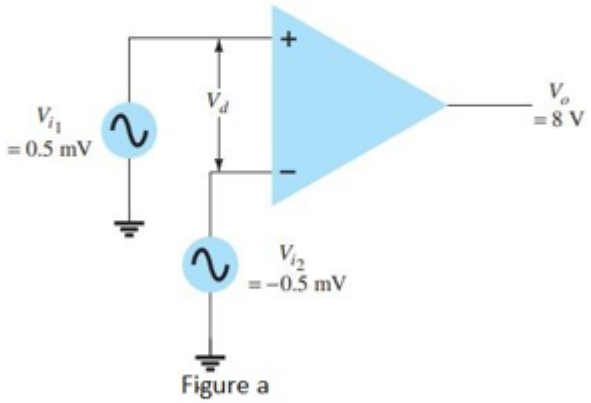


Figure a

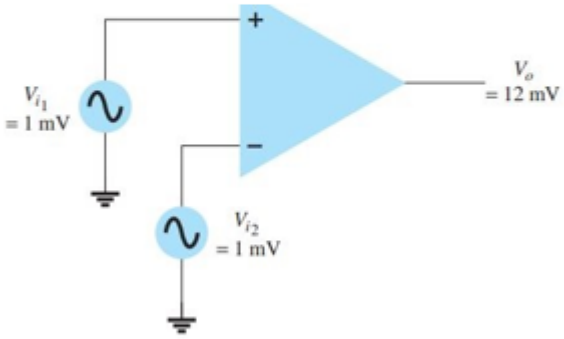
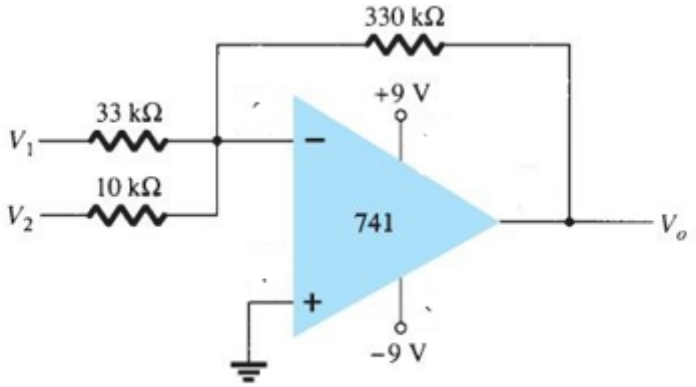


Figure b

c. Calculate the output voltage for the circuit of Figure. The inputs are $V_1 = 50mVSin(1000t)$ and $V_2 = 10mVSin(3000t)$ *(05 Marks)*

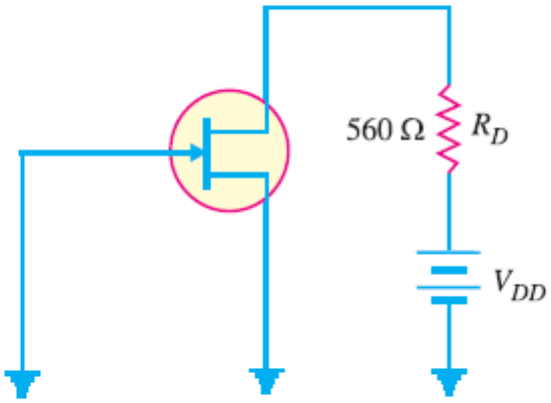


d. Design a circuit of non-inverting amplifier with a feedback resistor of 40kΩ that can produce amplification of 40dB. *(05 Marks)*
e. *Deduce the value of the input résistance if the* resistor of 40kΩ is replaced by a resistor of 2kΩ . *(03 Marks)*

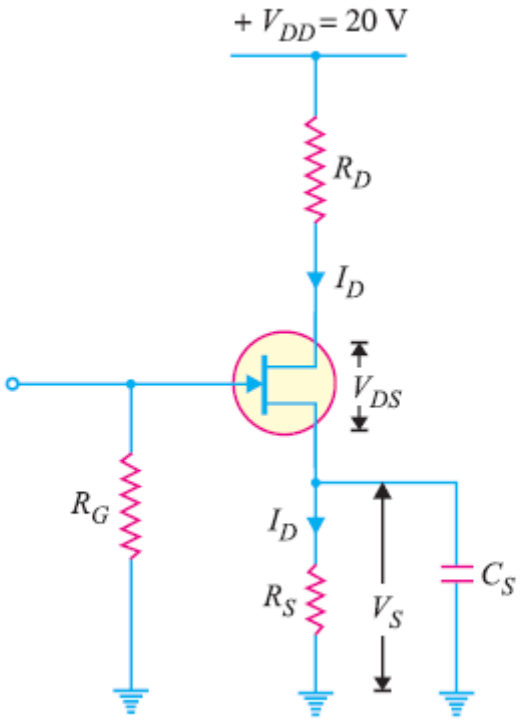
Section B Attempt any 2 questions in Section B

Question 1:

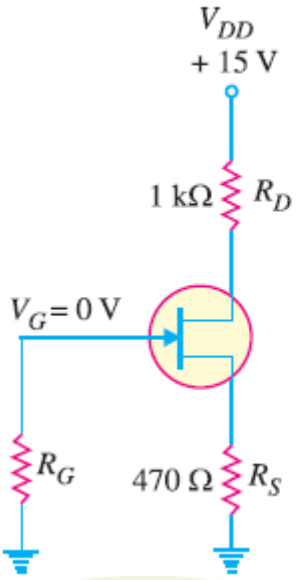
a. For the JFET in Fig. 2, $V_{GS\,(off)} = -5V$ and $I_{DSS} = 15$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation. (10 marks)



b. In a self-bias n-channel JFET, the operating point is to be set at $I_D = 2.0$mA and $V_{DS} = 10$ V. The JFET parameters are $I_{DSS} = 5$mA and $V_{GS\,(off)} = -2$V. Find the values of R_S and R_D. Given that $V_{DD} = 20$ V. (15 marks)



b. Find V_{DS} and V_{GS} in Figure below, given that I_D = 5mA (10 marks)



Question 2:

a. State any two applications of FET in electronic Engineering (02 marks)
b. Draw illustration diagrams to show symbols for both the MOSFET and JFET (02 marks)
c. Outline the 03 (three) advantages of FET vs BJTs (03 marks)
d. Sketch the characteristic and transfer functions of an FET indicating all relevant regions (10 marks)
e. Explain the following parameters as applied to FETsV_{pinch},V_{DS}, I_{DSS} (06 marks)

Question 3:

a. State the different types of Field Effect Transistors (04 marks)
b. How do Field Effect Transistors differ from Bipolar Junction Transistors (04 marks)
c. Explain why FET have gained massively importance in the electronics engineering lately (02 marks)
d. Sketch a schematic diagram of an n-channel FET illustrating all relevant terminals (05 marks)
e. By use of diagrammatic illustrations, explain the working principle of an n-channel FET (10 marks)

Question 4:

a. Determine ID and VGS for the JFET with voltage-divider bias in Figure below, given that V_D = 7V (15 marks)